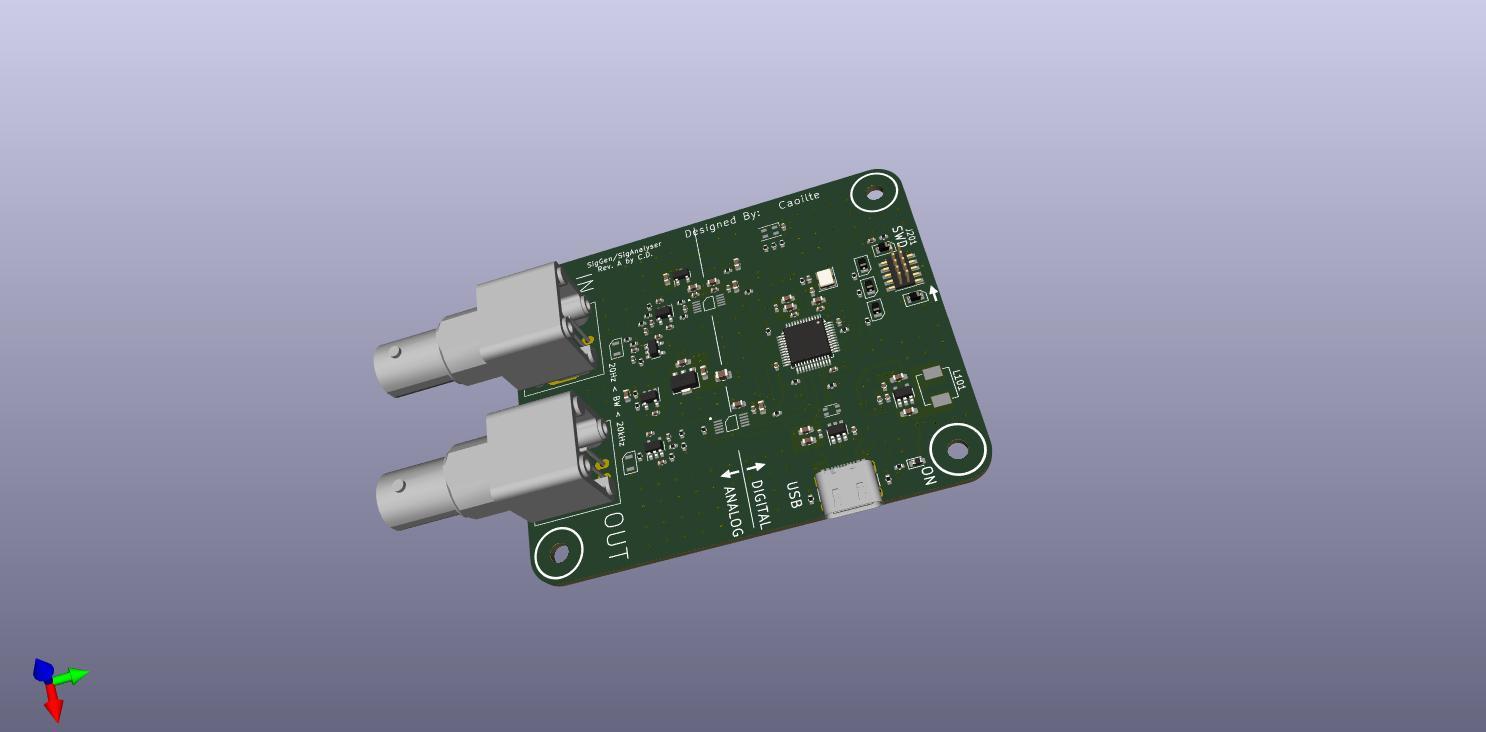
STM32 Mixed Signal Design:

Description:

The purpose of the presentation is to show the design considerations for a mixed signal board. The design contains low-frequency analog and high-frequency digital design elements on a 4-layer FR4 PCB. It will also include system-level design, component selection, analogue (e.g. op-amps, filters, ADC/DAC interfaces), digital (e.g. microcontrollers, USB), and power supply (e.g. switching converter) circuitry design, simulation, and schematic capture.



SYSTEM REQUIREMENTS:

**USB**

* The design is **low-frequency** (or low-bandwidth), 20 Hz to 20kHz approximately.
* The Max frequency of interest is 20kHz, so due to **Nyquist**, I need to sample at double the maximum frequency of interest.
* Sampling rate at least **40kHz**.
* To reduce quantisation error and get accurate readings I will need an **ADC with a minimum bit depth of 12**.
* Single channel data-rate: I Channel x 12 bits x 40,000 samples per second (fs=40kHz) = **0.46 Mbit*/s***
* USB 2.0 with• FS: up to 12 Mbits/s and HS: up to 480 Mbits/s → FS is more than sufficient!

* The system is a bus-powered device only (not acting as a host), therefore far less than 500m*A* current consumption.
* I Choose **USB Type C** as it is the newest tech.

POWER SUPPLIES

**Split digital and analogue supplies.**

Digital: **switching supply for efficiency**, digital is far more tolerant of noise. This digital circuit digital draws 100s of mAs maximum.

Analog**: linear (LDO) regulators for improved noise performance.** Analog circuitry typically draws less current (10s of mAs maximum) → regulator efficiency is not much of an issue.

**Input power from USB.**

* **(*V*ery) noisy power rail** → Requires adequate filtering.
* **Nominally +5V.** Can go as low as +4.5V → Watch out for regulator drop-out voltages!
* **150mA approx.**

Analog Sections:

**For ADC:**

• High-impedance (>I MOhm?) input buffer with ESD protection, RF filtering.

• Anti-aliasing filter with a cut-off at (max.) half the ADC sampling rate (Nyquist limit).

**For DAC:**

• Low-impedance (-50 Ohm?) output buffer with ESD protection to drive loads.

• Anti-aliasing filter with a cut-off at (max.) half the DAC sampling rate (Nyquist limit).

MISCELLANEOUS

**Mechanical**

• PCB dimension constraints, mounting holes, connector placement, which case are we designing for (conductor?)?

**Connectors**

• Debugging interface, input*/*output connector types (SMA, BNC, etc...).

**Peripherals**

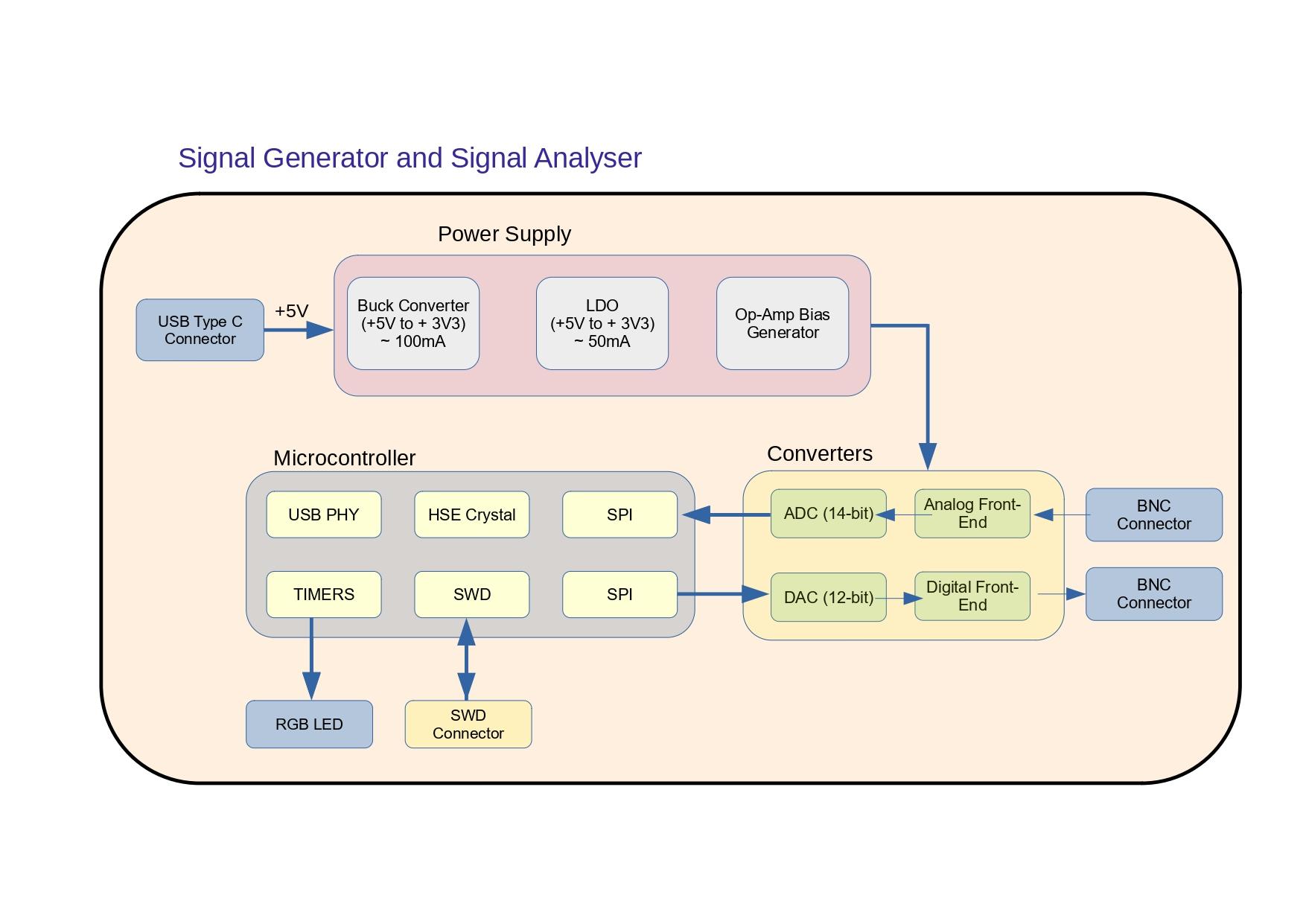
• LED to indicate power on, LED(s) connected to MCU for status information.

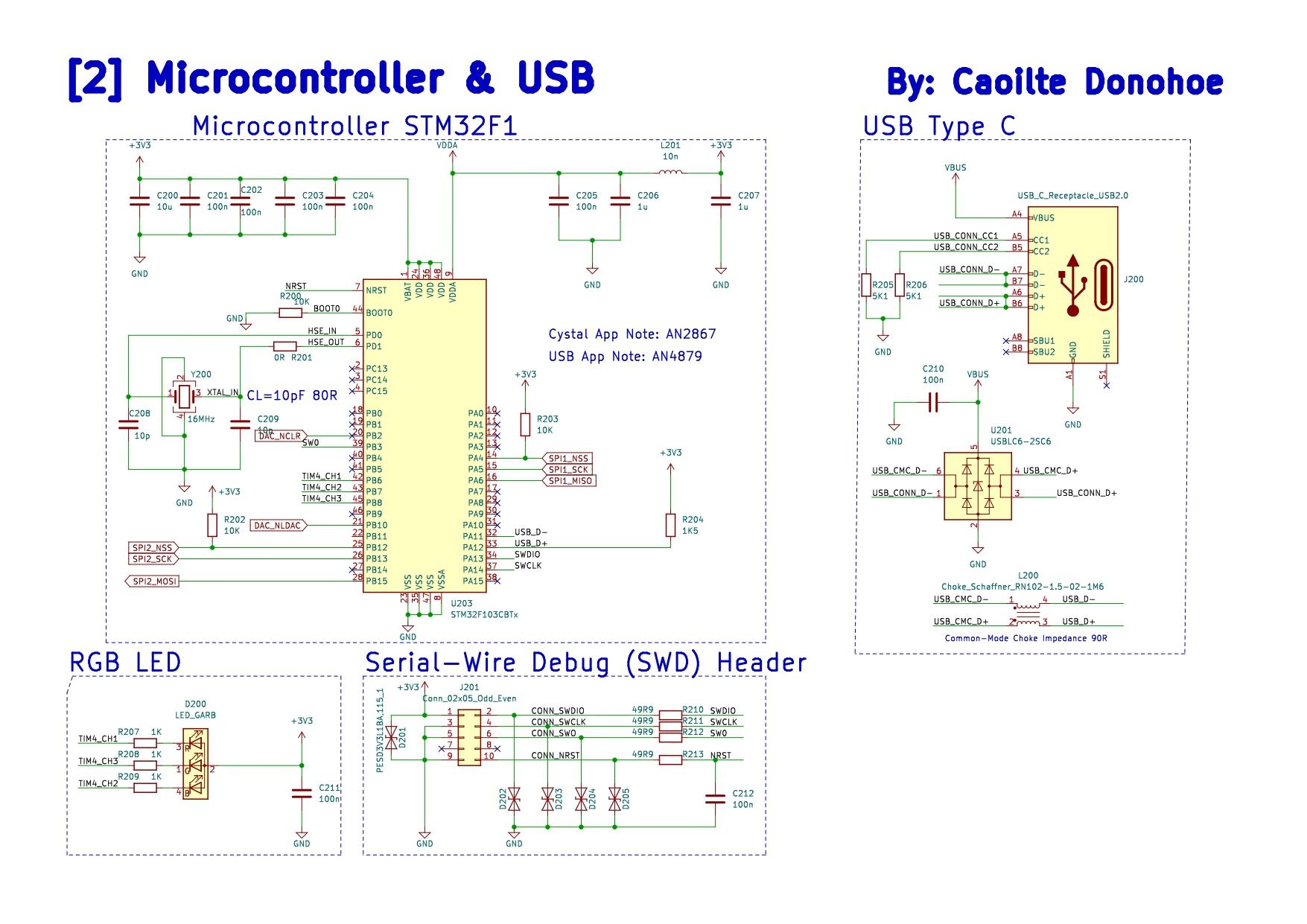
**Other**

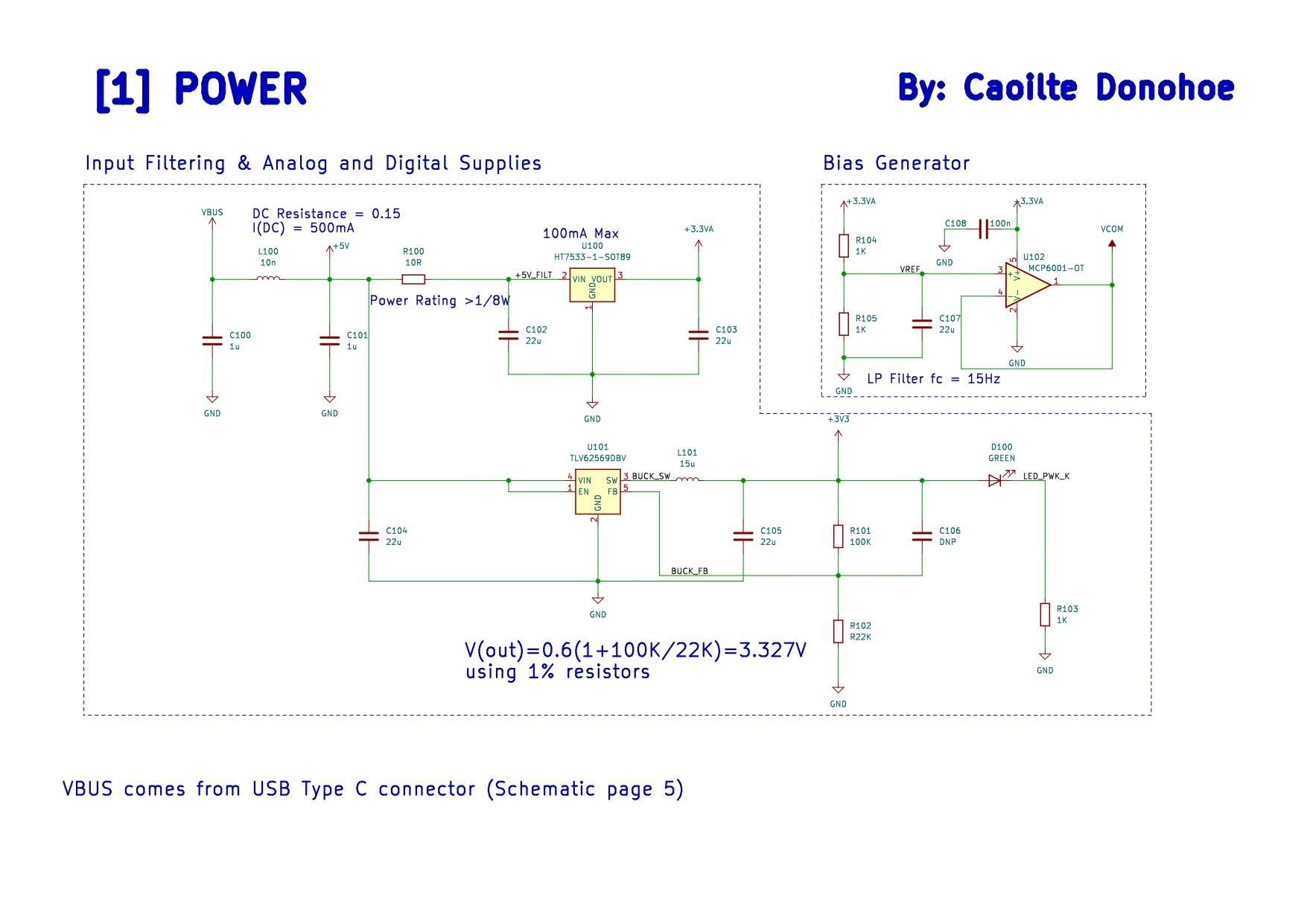
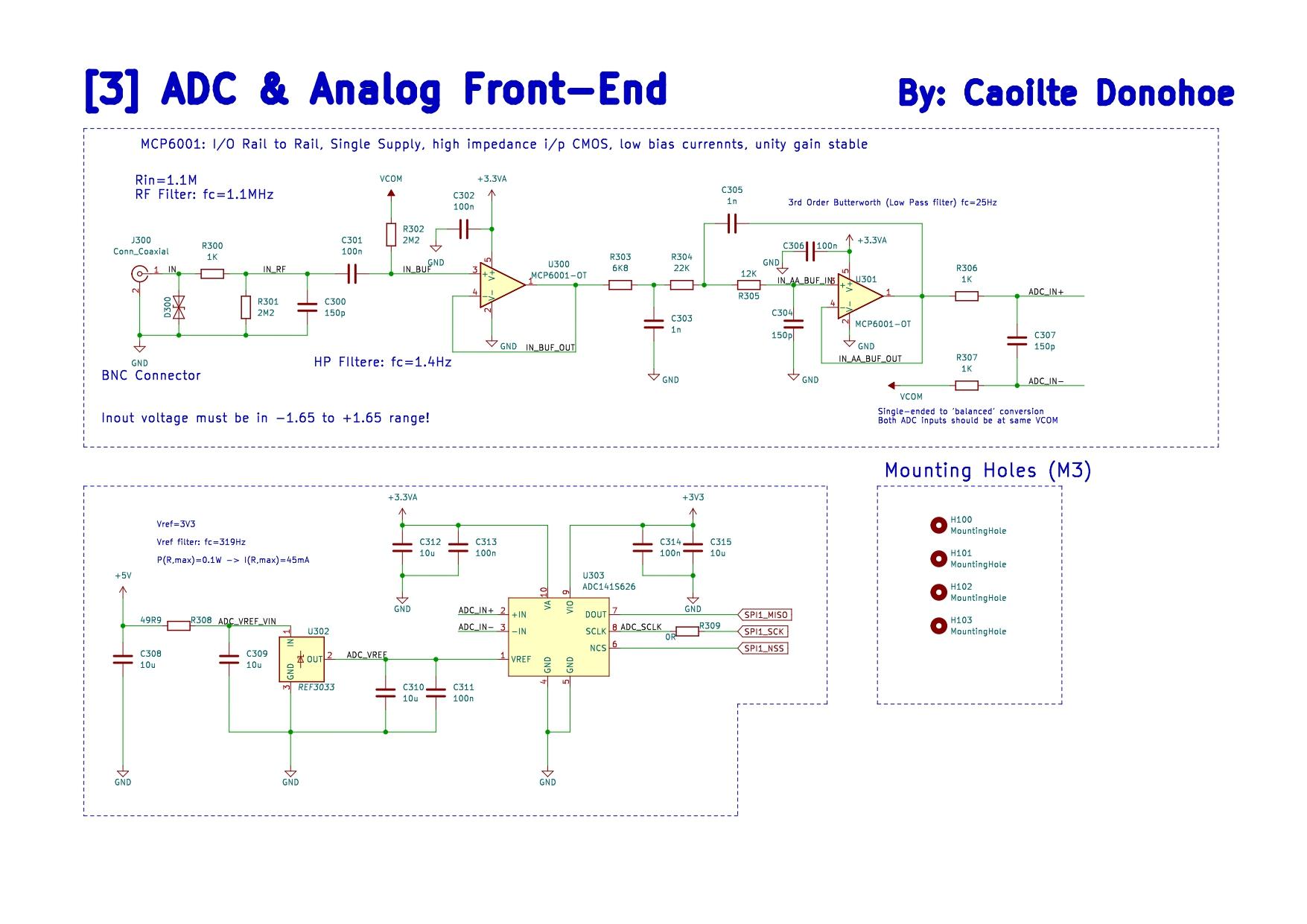
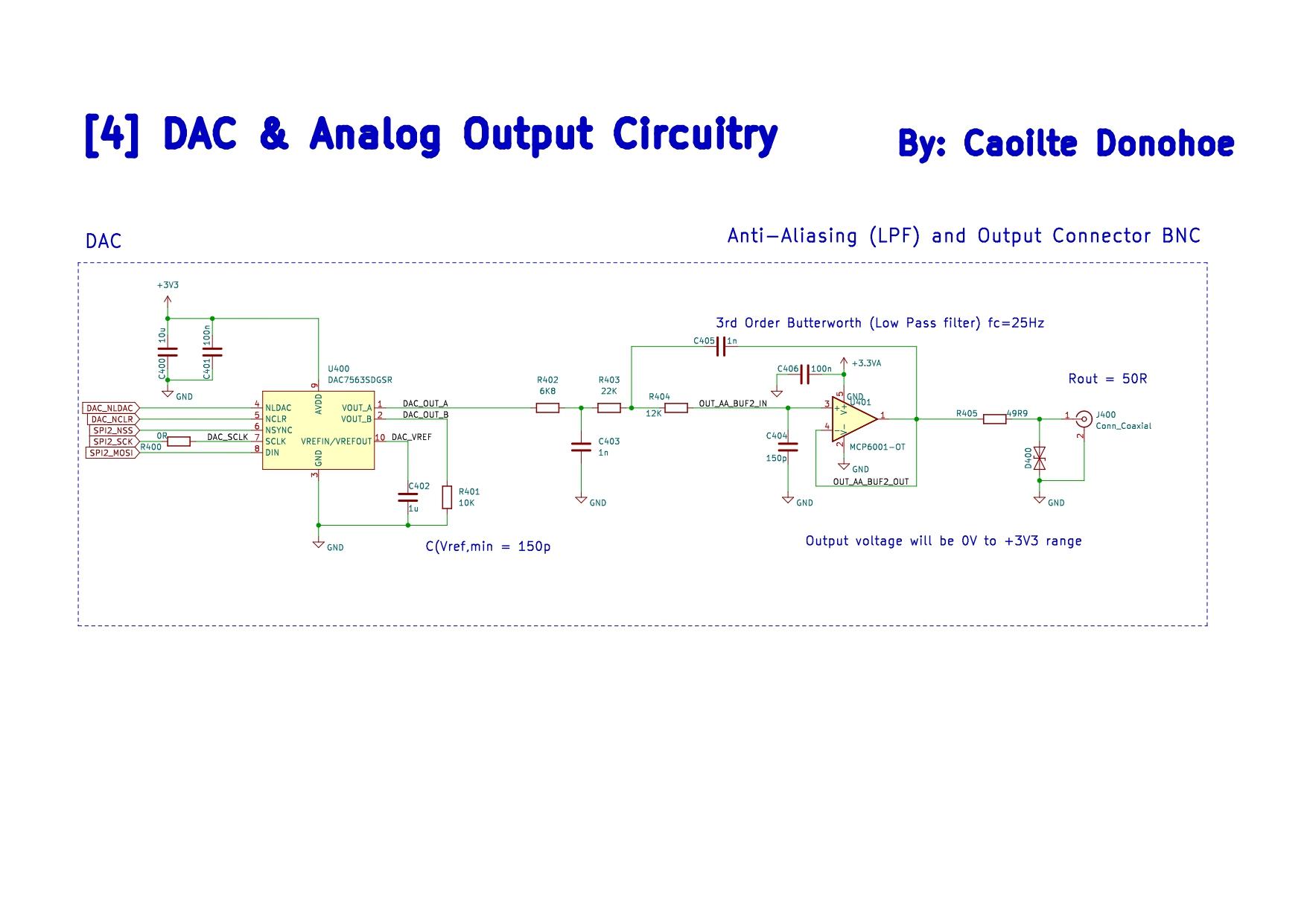
• Timing (crystal frequencies, types, etc...).

• ESD protection and filtering for EMC.

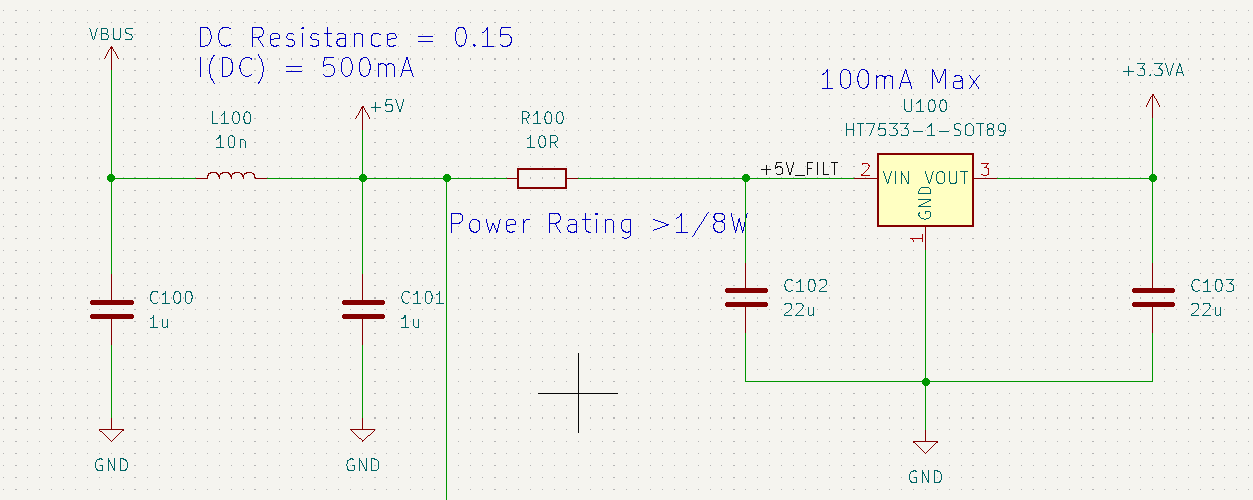
• Biasing for single-supply analogue circuitry.



Schematic Capture:

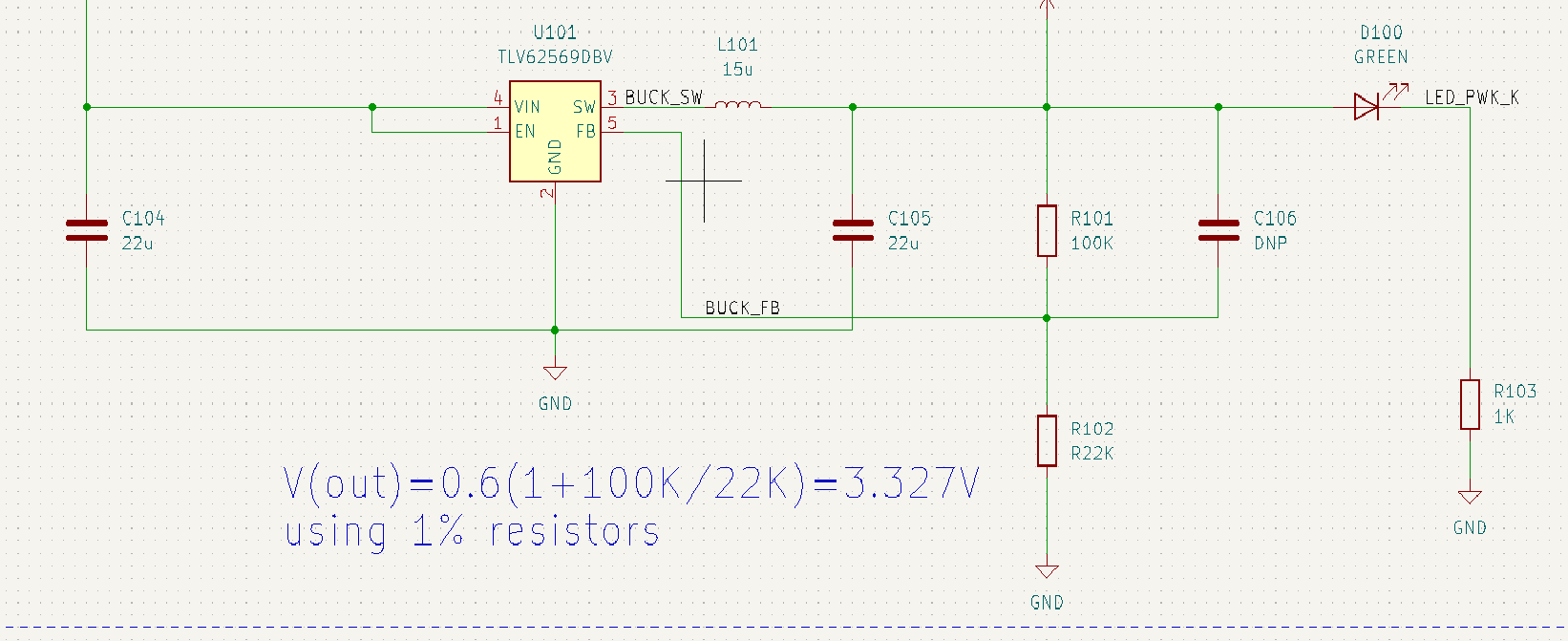


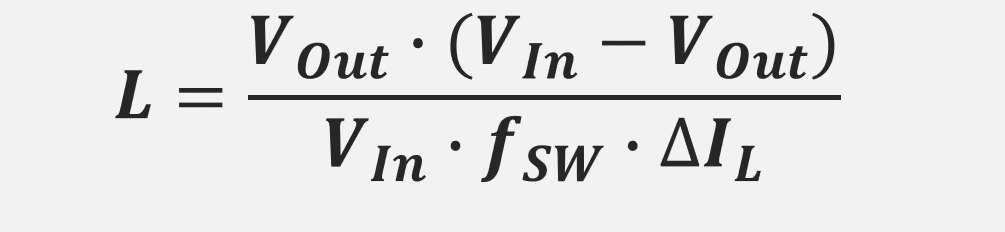
Schematic Design:

INPUT FILTER/LDO regulator

|  | |  | | --- | |  | |
| --- | --- | --- | --- |

INPUT FILTER/LDO regulator





**Inductor Calculations:**

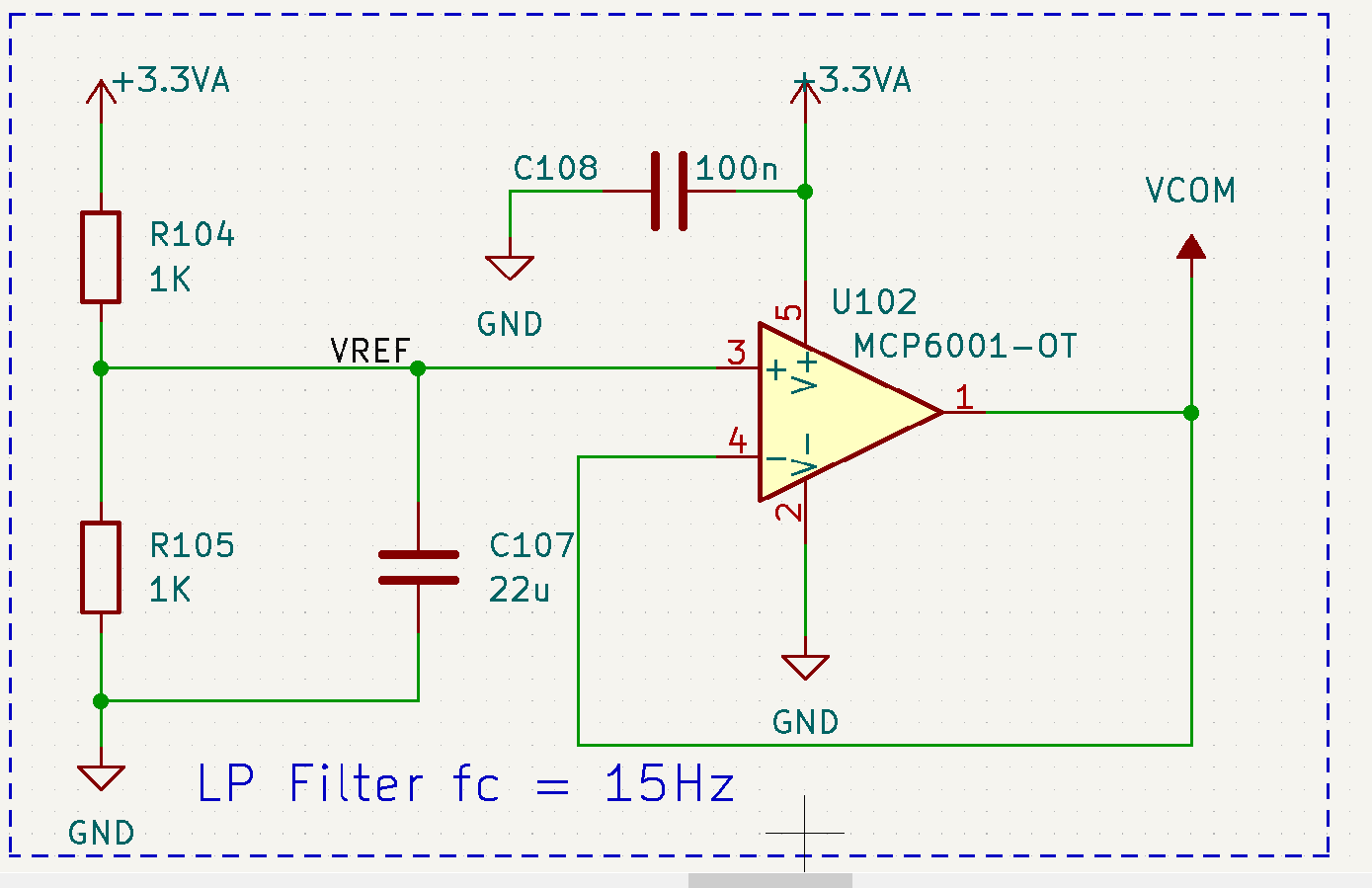
Vout = +3V3, Vin = 5V

fsw = 1.5MHz and Imin = 55mA

IL = 0.25 x 0.25A =0.1375

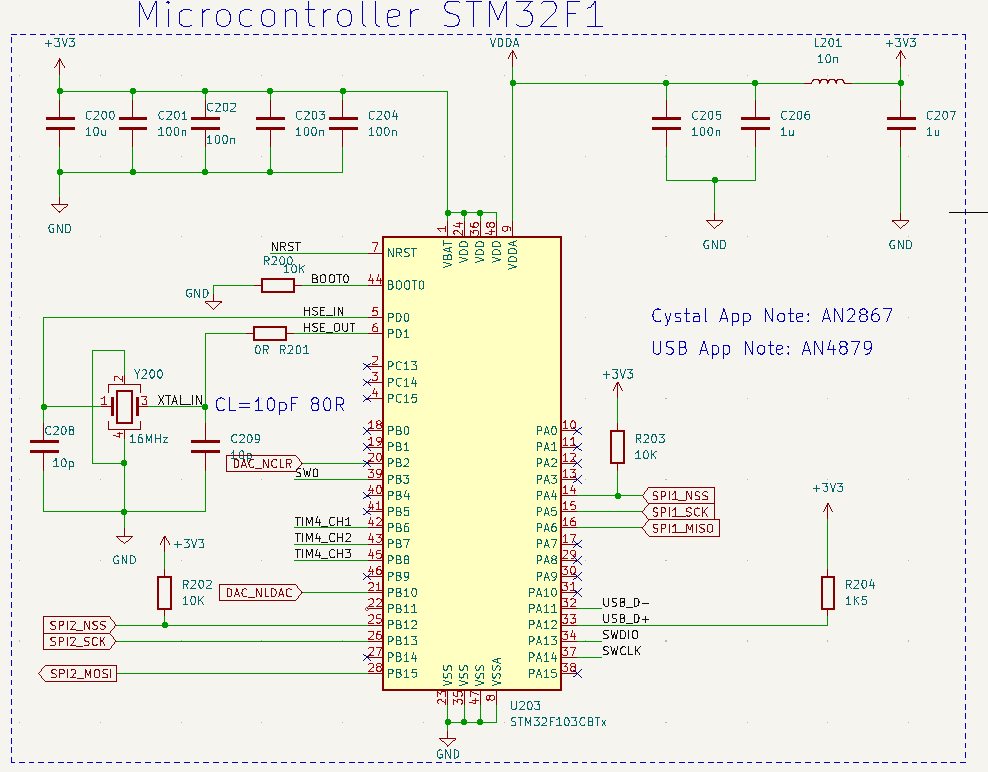
**Therefore L = 68uH**

BIAS GENERATOR:

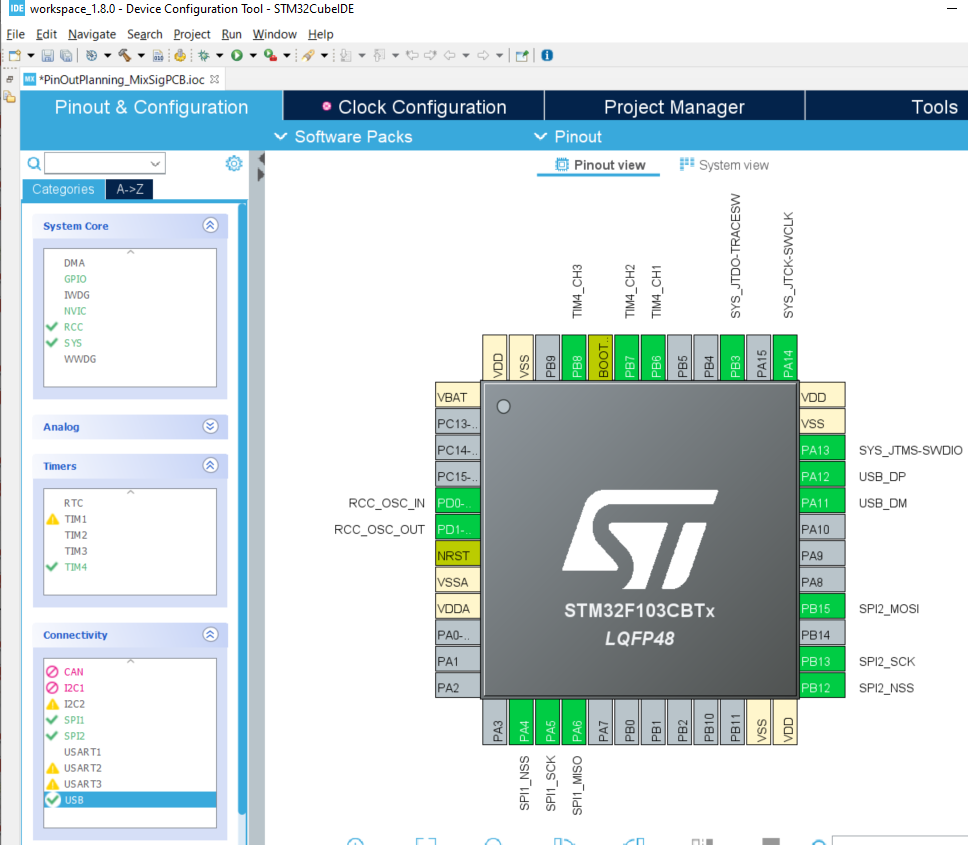


* Biased at VCC/2 to allow for FSD
* AC Signals are coupled onto Bias Gerator vial coupling caps
* Low Pass Filter via R105 and C107
* 3dB bandwidth = 15Hz

MICROCONTROLLER STM32F103:



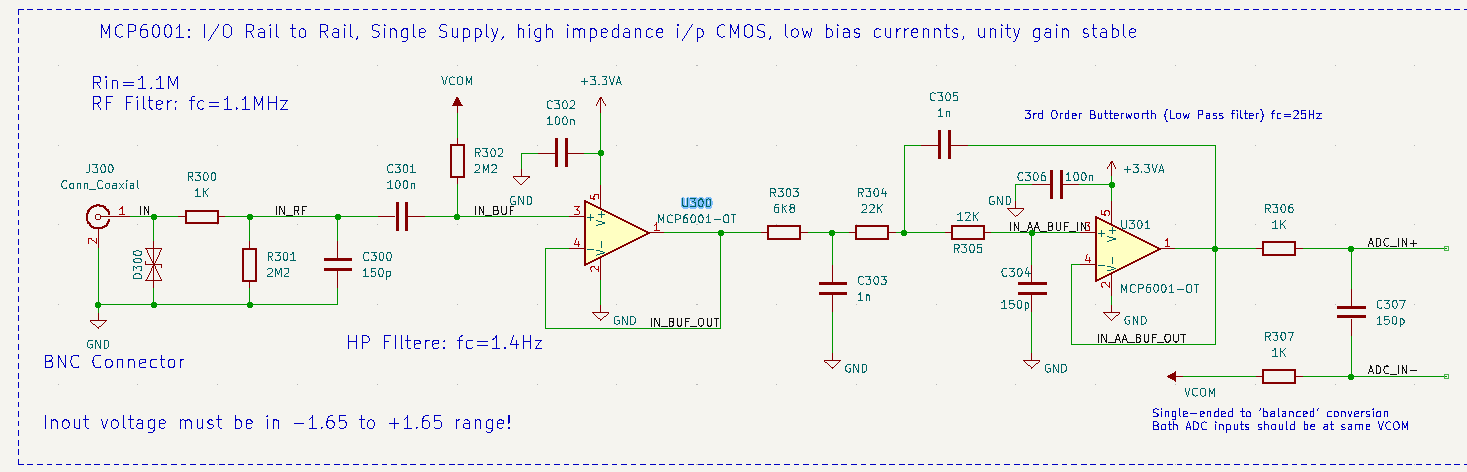
Pin Configuration and Function Assignment in STM32CUBEIDE

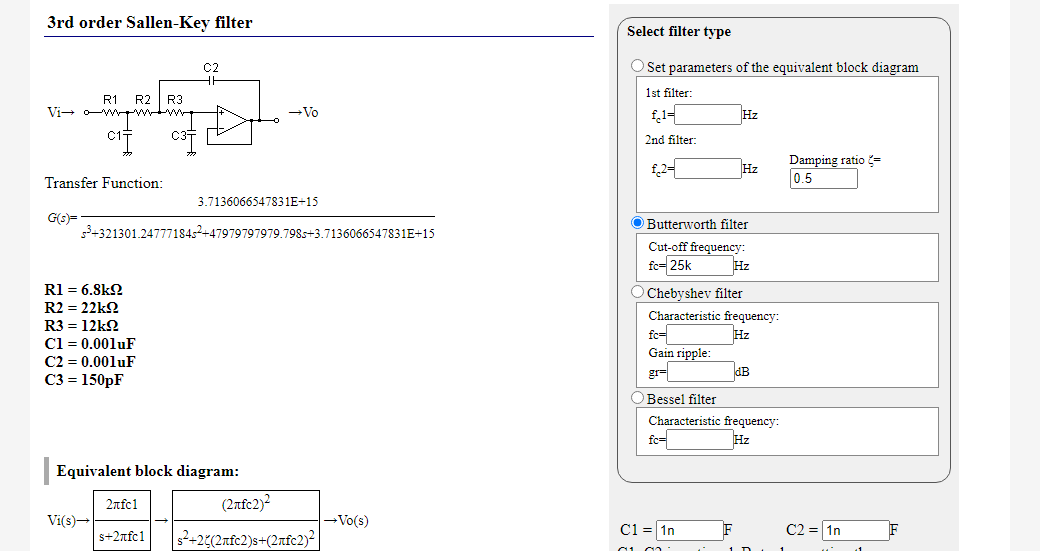


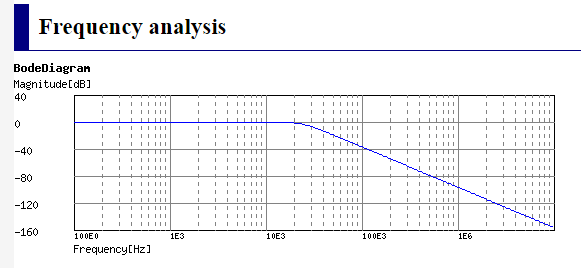
USB, ESD Protection and Filter for EMC:

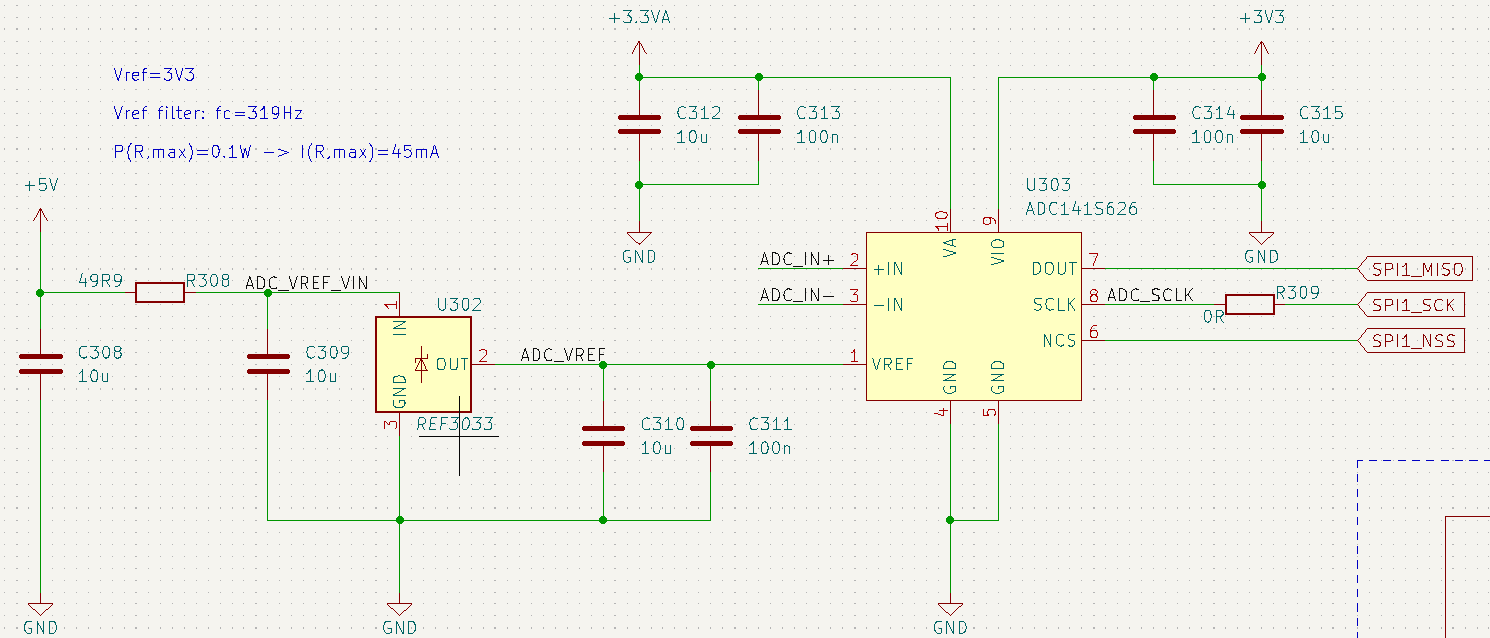
| * STM32F103 requires 1.5k pull-up on D+ Line * USB supply is noisy → Adequate filtering! RLC * Add ESD protection * Data Line Filtering → Optional via common mode choke to improve EMC performance * Tie CC1 and CC2 to ground for 5V 500mA power * ESD via Bi-Directional TVS diode |  |
| --- | --- |

ADC and Analog Front-End:

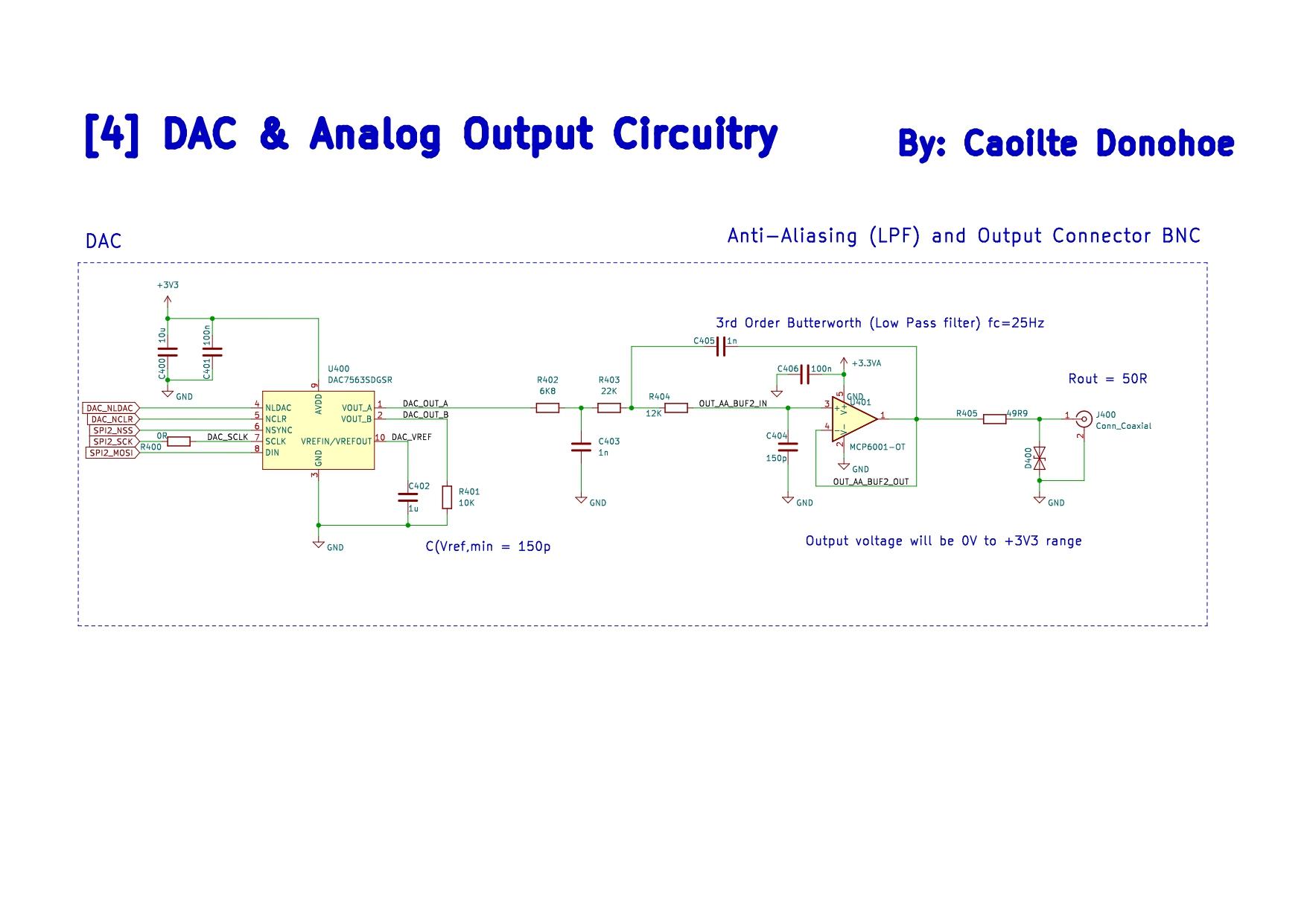






ADC Circuit:

Key parameters:

**Resolution (Bits)** 14 **Number of input channels:**  1 **Sample rate (Max) (kSPS)**: 250 **Interface type** : SPI **Architecture:** SAR

Key parameters:

**Resolution (Bits):** 12 **Number of DAC channels:** 2 **Interface type:** SPI

**Output type:** Buffered Voltage **Features:** Low Power, Reset to Mid-Scale, Small Size

**ADC Circuit:**

Q. Vref why use it?

1. To give more stability over temp and far greater accuracy and lower noise that ldo reg

Q. R308 what is it used for?

1. It is used to limit the current to I i/p max of 45mA

Q. What is R309 used for?

1. This can be placed with a slightly higher value to reduce ringing and improve EMC.

Note: Use Analog supply voltage for Analog side. Use Digital Supply for digital supply. The IC is split in half, the analog pins to the left and the Digital pins to the left.

Also do not split the ground pins. They should be on the same plane

Analog Front-End: **First stage**

Q. What is the TVS diode for?

1. The TVs diode is used to protect the circuit from ESD. It is bi Directional as the signal swings between +ve and -ve

Q. Input filter is it high pass or low pass and what are the components used?

1. The input filter uses R300 and C300 as a low pass filter with a cut-off freq 1.1MHz from say FM radio or WiFi etc

Q. Calculate the I/p impedance

1. I/p impedance is the parallel of R301 and R302 or 2.2Meg || 2.2Meg or 1.1 Meg

Q. What is C301 used for?

1. It is an AC coupling cap or dc decoupling cap. +1.65V to -1.65V

Q. What is Johnson Noise?

1. High-value resistors in the source path generate noise. Keep these values low. R301 and R302 are not in the path but parallel to it i.e. they have a path to ground.

Q. What is Vcom?

1. Vcom is the DC bias voltage. It is set to be half the Vcc or 1.65V. This allows an AC signal of +1.65v to -1.65 volts

Q. Describe the op-amp?

1. CMOS op-amp, high impedance i/p, low impedance o/p, unity gain, voltage follower. With CMOS op-amps you have low i/p bias currents. High Z so it won't load the sensor or i/p.
2. It reduces aliasing artefacts due to sampling.

**Second Stage: Sallen Key**

Q. What are its features?

1. 3rd order (3 caps) Butterworth filter, LPF , maximally flat, unit gain LPF

Q. What is its function?

1. To prevent aliasing therefore an anti-aliasing filter.

Q. Controlled impedance over what conditions?

1. Over frequency, the impedance of the circuit would fluctuate. With an active filter, this won't happen.

Q. Why choose lower-value resistors?

1. You get Johnson noise with high-value resistors that are in the signal path. Calculate passive components with higher value caps in C305 and C306 (1nF). The values for resistors will be lower.

**ADC Circuit:**

Q. Where is the Voltage Ref?

1. The voltage ref is built in

Q. Explain the filter?

1. Filter Salen key is the same as ADC but its a reconstruction filter

Q. What is the output of the op-amp

1. Output from DAC is analog and it biases the the op-amp. So it will be from 0 to 3.3V as it is rail to rail.

Q. What is R405 used for?

1. The output from the op-amp is very low and unstable so it defines the output impedance